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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,179	04/19/2004	Chih-Huang Chang	10544-US-PA	3178
31561	7590	07/10/2006	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			HA, NATHAN W	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 07/10/2006

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/709,179  
Filing Date: April 19, 2004  
Appellant(s): CHANG ET AL.

\_\_\_\_\_  
Linda Lee  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 4/12/06 appealing from the Office  
action mailed 10/13/05.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15-16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ono et al. (US 2003/0107129, previously cited, hereinafter, Ono.)

In regard to claim 15, in fig. 2, Ono discloses a method of fabricating bumps on a chip, the process comprising:

providing a chip 15 with an active surface (top surface) having a plurality of bonding pads 16 thereon and a backside (bottom side.)

forming at least a bump pad 14 on the backside of the chip; and

forming a bump 19 to the bump pad.

In regard to claim 16, Ono further discloses forming a metallic layer 14 or 21 on the backside of the chip; and

patterning the metallic layer to form the bump pad (figs. 11c and 11d show this step.)

In regard to claim 18, Ono further shows forming the protective element 18 on the active surface of the chip.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Akram (US 6,861,763, previously cited.)

In regard to claims 17 and 19, Ono discloses all of the claimed limitations as mentioned above except the mask has at least an opening so that the backside of the chip is exposed.

Akram, in fig. 6A, discloses an analogous package includes chip 12 pad 14, mask 30C wherein mask layer, or passivation layer, has an opening so the chip is exposed and forming a metallic layer 14 over the mask and the exposed portion of the

chip. This opening further provides access to the to the chip for electrical connections. The mask or passivation layer then further removed to form a solder ball therein.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize opening portions on the chip in order to provide electrical connections.

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Koh (US 2004/0135266, previously cited.)

In regard to claim 20, Ono discloses all of the claimed limitations as mentioned above, except using a wire-bonding machine in the process of making the electrical connection elements, bond pad, for example. It should be noted that wire bonding is widely used in the semiconductor package to form wire connections, bonding pad, and solder balls since it is widely available and provides easy access to such small area on the chip.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize the method as taught by Koh in order to facilitate the method of forming electrical connection elements.

#### **(10) Response to Argument**

In regard to claims 15-16 and 18, the Appellant contends that Ono, '129, does not teach the limitation of forming a bump pads on the backside of the chip because they are formed on a dielectric layer, instead.

The above argument is not found persuasive. First, it should be noted that the conductive pattern 14 of the cited prior art is the same as a conductive pad, or bump pad, since they function the same as providing electrical connections between devices. In semiconductor packaging, a metal connection pad is usually called a bump pad. In this case, the pattern 14 of the cited prior art is characterized as a bump pad since it provides electrical connections between the bump 19 and the semiconductor chip 15 through the intermediate element 13. Figure 2, for example, shows that the chip 15 has an active surface (top surface) including at least a bonding pad 16, and the backside, which is formed opposite to the active surface. Appellant argues that the pattern 14 cannot be formed on the semiconductor chip 15, or vice versa.

However, figures 2-3 of Ono, show otherwise. Figure 3 is a bottom view of the package; it shows that element 13 formed inside the area where the chip 15 is formed on. This indicates that the chip must be formed on the at least portion of the pattern 14 on the backside and within the perimeter of the chip since element 13 is directly connected to the pattern 14 at one end as shown in figure 2. Therefore, Ono indeed discloses the pattern 14 formed on the backside of the chip 15. Ono further discloses that the bumps 19 are arranged in an array on almost the whole area of the bottom surface of the semiconductor device 15. See paragraph [0029].

Appellant appears to interpret the meaning of the prior art's teaching in paragraph [0029] different than what it actually means. Portion of paragraph [0029] states that pattern 14 located above the through hole and formed on an area other than the area where the chip is mounted. This means portion of the pattern 14 protrudes

outside of the area where the chip is mounted. It is clearly shown in figure 3, where one end of the pattern 14 protrudes out of the bottom of the chip in order to provide connection the wire 17. The bottom of the chip is obviously not formed on this protruded portion of pattern 14. Ono further describes that metal bump 19 is formed on the whole area of the bottom of the chip, and since metal bump 19 is also formed on the pattern 19; it is clear that pattern 14 is formed on the bottom area of the chip.

Appellant further submits that Ono is silent about forming a bump on the bump pad (in appeal brief, page 6). It is not clear which limitation in the phrase "formed on" that the Appellant refers to. Phrase "formed on" includes limitation "formed" and limitation "on". In a method claim, the "formed" may be given a patentable weight if it is described explicitly in the specification. In this case, the Appellant's specification merely discloses that "formed" is a step which the chip and the bump pad are put together. There is no specific step of method stated otherwise. The "on" limitation is used to describe a relationship, or position, of an element, which physically relates to another. It appears that the Appellant mischaracterizes the term "formed on". In general, this whole phrase refers to a position of a subject related to another and it does not exclude anything in between. With this in mind, the bump 19 is indeed formed "on" the pattern 14 through the device 13, as clearly shown in the cross section of figure 2. The Appellant admits that the bump is formed "on" only pattern 11 and not element 14. It appears that the Appellant refers to "directly formed on". It is true that the bump 19 is not "directly formed on" the element 14; however, the claim does not explicitly require the bump to be formed "directly on" the pad. Therefore, the limitation as mentioned is



still taught by Ono. It should be further noted, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In regard to the argument of the 103 rejection of Ono and Akram, Appellant argues that there is no mask layer formed on the back side of the chip. This is not found persuasive since Akram indeed teaches the mask layer 30C on the backside of the chip, or die, 12 as a protection layer (col. 8, lines 25-50). The Appellant seems to suggest that the claim requires the order of the steps sequentially. However, the claim language does not require the steps of forming the device in sequence since the term "comprising" is inclusive.

Furthermore, paragraphs D4 and E4, pages 8 and 9, repeat that neither Ono nor Akram discloses at least a bump pad on the backside of the chip and forming a bump on the bump pad. These limitations are addressed above regarding to claim 15.

For the above reasons, it is believed that the rejections should be sustained.

The Examiner wishes to point out that the serial number appear in the header of each page of the Appeal Brief is incorrect.

Respectfully submitted,

Nathan Ha



Conferees:

Ricky Mack



Wael Fahmy

